## AMENDMENTS TO THE CLAIMS

Please add or amend the claims to read as follows, and cancel without prejudice or disclaimer to resubmission in a divisional or continuation application claims indicated as cancelled:

1. (cancelled) A method of storing bits on a Non-Volatile Memory ("NVM") array comprising: receiving a block of bits in a specific order; rearranging the order of the bits in the received block according to a spreading pattern; generating an error correction code ("ECC") based on either the original block of bits or based on the rearranged block of bits; and storing in said NVM array the ECC and the block of bits from which the ECC was not derived.

2. (cancelled) A method of reading a block of bits stored in a rearranged order according to a spreading pattern on a Non-Volatile Memory ("NVM") array comprising: rearranging the stored block with an inverse-spreading pattern and manipulating the block with an error correction code ("ECC") generated prior to the block being rearranged according to a spreading pattern and stored.

3. (cancelled) A method of reading a block of bits stored on a Non-Volatile Memory ("NVM") array along with an error correction code ("ECC"), which ECC is based on the block of bits after being rearranged by a spreading pattern, said method comprising: rearranging the stored block with the spreading pattern and manipulating the rearranged block with the stored ("ECC"); and rearranging the manipulated block of data with an inverse-spreading pattern.

4. (currently amended) A control circuit for storing bits of a data block on a Non-Volatile Memory ("NVM") array, said circuit comprising:

   a bit scrambling block adapted to rearrange the bit of the data block according to a spreading pattern;

   an Error Correction Coding ("ECC") block adapted to generate an ECC based on either the original data block or on the rearranged data block; [and]

an NVM storing circuit adapted to store in said NVM array the ECC and the block of bits from which the ECC was not derived[.];

a reading circuit adapted to read a stored block of bits from the NVM array;

wherein said bit scrambling block is adapted to scramble the read data block if the block was stored unscrambled; and

wherein the ECC block is adapted to manipulate the scrambled block according to an ECC which is based on a scrambled version of the original data block prior to being stored on the NVM.

5. (cancelled) The control circuit according to claim 4, further comprising a reading circuit adapted to read a stored block of bits from the NVM array.

6. (currently amended) The control circuit according to claim [5] 4, further comprising a de-scrambler adapted to rearrange a block of bits stored according to spreading pattern.

7. (original) The control circuit according to claim 6, wherein the ECC block is adapted to manipulate the de-scrambled block of data according to an ECC which is based on the original data block prior to scrambling.

8. (cancelled) The control circuit according to claim 5, wherein said bit scrambling block is adapted to scramble the read data block if the block was stored unscrambled, and wherein the ECC block is adapted to manipulate the scrambled block according to an ECC which is based on a scrambled version of the original data block prior to being stored on the NVM.